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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,084	03/04/2002	Donald C. Soltis JR.	10016691-1	5905

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,084	SOLTIS ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticpated by Gupta (patent No. 5,999,736).

1. Gupta taught the invention as claimed including a data processing ("DP") system comprising: processing like instructions (instructions that were like in one or more attributes e.g., from the same programming language or performed similar functions or accessed the same hardware) through two or more instruction paths of the processor, each of the paths having a different heuristic (e.g., see col. 26, lines 20-43); monitoring progress of the first like instructions through the instruction paths (e.g., see col. 26, lines 20-43); determining which of the instruction paths is a first leader in processing the first like instructions (e.g., see col. 26, lines 20-col. 27, line 50); modifying the heuristics of one or more of the instruction paths based on the heuristics of the first leader (and the heuristics of the non-leaders) with respect some processing attribute such as resource utilization and memory latency (e.g., see col. 26, lines 44-col. 27, line 50).

2. As per claim 2, Gutpa thought like instructions comprising as a bundle from a common thread (e.g., see fig.12, col. 24, line 5-col. 25, line 24, and col. 26, lines 25-53).

3. As per claims 3,4 Gupta taught modifying comprising modifying heuristics of each of the execution paths (e.g., see col. 26, line 20-col. 27, line 50).

4. As per claim 5, Gupta taught processing the first like instructions through the leader without being affected by modifying (e.g., before the modifying is performed) (e.g., see col. 26, line 20-col. 27, line 50).

5. As per claim 6, Gupta taught processing additional instructions from a program thread of the first like instructions through the multiple instruction paths without redundancy (e.g., using classes of instructions and path signatures) (e.g., see col. 24, line 42-col. 25, line 24).

6. As per claims 7,8,10 Gupta taught processing further groups of instructions in the manner the first like instructions were performed wherein the two or more instruction paths of the process had different heuristics and the second like instructions were monitored determining which of the instruction paths was the second leader an modifying the heuristics of the second leader and of the non-leader where the heuristics comprised CPU bound heuristics such as floating point execution unit utilization and memory bound heuristics such as memory utilization (e.g., see col. 26, line 20-col. 27, line 50).

7. As per claim 9, Gupta taught modifying heuristics based upon one or more of branch prediction and prefetch heuristics (e.g., see col. 27, lines 11-30 and col. 24, lines 5-34).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 11-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore (patent No. 6,715,062) in view of Gupta (patent No. 5,999,736).

9. Moore taught the invention substantially as claimed including a data processing ("DP") system comprising: at least two parallel instruction paths each of the paths having an array of pipeline execution units and associated heuristics affecting how the instructions are processes therein (e.g., see fig.1) and logic to assess for monitoring the processing of instruction with the paths (e.g., see col. 6, line 40-col. 7, line 35).

10. Moore did not expressly detail (claims 11,14,15,16,18,19,20) modifying the heuristics of one of the paths to improve thread performance. Gupta however taught monitoring like instructions and modifying the heuristics of paths for improve thread performance and repeating the procedure for further threads (e.g., see col. 26, line 20-col. 27, line 50).

11. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Moore and Gupta. One of ordinary skill would have been motivated to incorporate the Gupta teachings of modifying the heuristics at least to provide better performance in instruction processing.

12. As per claim 12, Gupta taught modifying heuristics based upon one or more of execution heuristics, cache heuristics and fetch heuristics (e.g., see col. 27, lines 11-30 and col. 24, lines 5-34).

13. As per claim 13, Moore taught the parallel instruction paths on a common die (e.g., see fig. 1 and col. 5, lines 7-36).

14. As per claim 17 Moore taught instruction paths forming a cluster and arranged in a manner to processing instructions in bundles (e.g., see fig.1). Gupta also processed instructions in bundles (e.g., see col. 26, line 20-col. 27, line 50 and col. 24, line 5-col. 25, line 24).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Adl-Tabatabai (patent No. 6,170,083) disclosed a method of performing dynamic optimization of compute code (e.g., see abstract and figs. 5 and 7).

Gustafson (patent No. 5,245,638) disclosed a system for benchmarking computers (e.g., see abstract).

Ball (patent no. 5,615,357) disclosed a system for verifying processor performance (e.g., see abstract).

Johnson (patent No. 6,748,589) disclosed a method for increasing speed of speculative execution (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER